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Test Algorithms for Embedded Systems Testing

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Abstract— Now a days, embedded systems are used in day to day life. Though people of all ages are using embedded system in daily life they are totally unaware about it. As it is widely used as safety critical device, Testing are the main issue and a matter of concern for the manufacturers.Embedded systems are developed against the issues such as best performance, less power and low cost. Several faults occur while running embedded systems. Some of them are related to components, some are related to memories and some are related to interfacing with hardwares. All these errors can be easily removed via testing algorithms.This paper focuses on new test algorithms for testing of memory of embedded systems. It deals with on online testing of embedded system and also describes the various testing techniques. BIST (Built in Self Test) which is widely used for non concurrent system is also discussed in this paper.

Index Terms— BIST, Non Concurrent System, Safety criticality.

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1 Introduction

Embedded system is a system which is used for a specific or dedicated application. It is widely used in daily life by people of all ages. The examples of embedded system ranges from toys used by small kids to automobiles and even household applications like washing machine and microwave oven. Embedded systems are also used for developing applications for social cause. When embedded systems are deployed in all these areas safety criticality becomes an important issue in front of designers and manufacturers. Since most of the applications of embedded system are mobile devices they are harshly used by the users. Toys can be mishandled by children. Automobiles are prone to extreme temperatures thus sustainability and reliability becomes an important issue. Before these systems are handled by the users they have to be tested in real time environment by assuming all possible criteria. Online testing of embedded system is one of the techniques to achieve reliability of embedded system in terms of its safety criticality.

2 Online Testing

Whenever there is a physical or logical defect in a device, a fault is said to have occurred. Faults may lead to error, incorrect result. If the results of such system are dependent on other factor which is severe it can get prone to hazards or mishap. The reason of fault in a system may differ from condition to condition. It can be fabrication fault with loose or open wire leading to shorts.

Fault may also arise in system due to exposures to extreme temperatures below sustainability of that IC, if it is too high or too low. Online testing is used to reduce operational faults in a system for safety critical devices. Redundancy is one of the important parameter considered in online testing. The cost of online system can go a bit higher as compared to other techniques since there is a need to keep extra hardware and software systems in case of faults.

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3 Need to Test Memory of Embedded System

The need to perform memory testing is to ensure that each memory location is in working state. Assume that a number 20H needs to be stored at a memory location 2000H. 20H should reside in that memory location until a new data is stored in same memory location. Testing is required to check whether the storage locations are getting updated by every write instructions. After every write instruction, a read instruction will check that new data is updated in storage. If all new write is updated then the system is said to have passed memory testing.

Hardware as well as software faults arise in memory.There is a great difference between software and hardware as hardware can be manufactured and software is logically developed. Testing of hardware is not similar to testing of software. Faults occurs in memeory are like leakage, wiring problems, interfacing problems, faulty chip problems and power related problems. In case of hardware the problems are difficult to handle because of complexity and critical structures. The faults occurs in hardware are stuck at faults bridging faults, stuck open and stuck short faults, spurious current fasults, Power disturbance faults, permanent faults, intermittent faults and transient Faults[12].

4 Built In Self Test

With the increase in need of storing more data, size of memory is increasing day by day. With increasing size the amount of time and number of test required are increasing as it is directly proportional to the size of memory. To achieve high reliability for efficient use of memory cores, memory has to be internally tested. Built in Self Test is one of the techniques used to test memory internally. With the help of BIST a system is not only capable of

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detecting faults but also finding the exact cause of fault for its early repair. BIST does not need to store testing data and timing restriction is insignificant [10]. The BIST approach was originally implemented to test embedded memories in the Atmel AT94K series SoC which consists on an embedded FPGA core, embedded memory cores, and an embedded Advanced Virtual RISC (AVR) processor with various peripheral units [11].

The diagrammatic representation of BIST can be given as shown below:

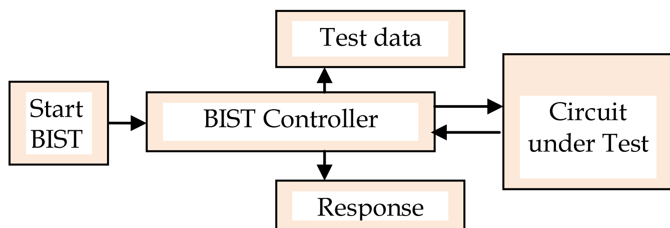


Fig.1. Working of Built In Self Test

5 Memory Testing of 8051 microcontroller

Embedded memory is any non-stand-alone memory. It is an integrated on-chip memory that supports the logic core to accomplish intended functions. High-performance embedded memory is a key component in VLSI because of its high-speed and wide bus-width capability, which eliminates inter-chip communication. During the past several years, a lot of development has taken place in the embedded memory market. Most recently, many new products were introduced with embedded memory. In this project work we are focusing on EEPROM memory for testing purpose. Several algorithm were developed that can detect only single fault and some of them are stuck-at fault model, transition fault model , coupling fault model , etc [4]. Further March algorithm was introduced that can cover 4 to 5 faults together. After special march algorithm were developed to detect coupling fault of RAM [7].

Early, to detect any fault from the above mentioned fault, respective fault model was used for example to detect stuck-at fault, we need to use stuck-at fault model, to detect delay faults we need to use delay fault model. Etc. Also Automated Test Equipment (ATE) can be used to test memory chips, boards, systems, during their final process. After Boundary-scan test was used. Then Built-in-self-test was introduced to overcome all the drawbacks of traditional fault model. BIST circuit is added internally to test the circuit. BIST can allow multiple testing, and it does not require ATE. But as it is present inside the chip, it uses area which not feasible [8]. March test is when a set of test instruction steps (normally is generated by LFSRs) are performed to test each cell of memory array in order [2].

Testing an embedded memory is quite difficult Means we cannot directly access the embedded memory. Now to test such memory we need to study functional diagram of embedded memory [5]. Further interfacing of embedded memory with our software is required so that we can send test cases. This serial interfacing of embedded memory is explained in [3].

The different types memory are explained in [6] some of them are listed bellow in details Stuck-at fault, transition fault, and coupling fault is relatively easily tested compared with NPSF.

- Stuck-at Fault Model: The logic value of memory is stucked at '0' or '1', and not changed.
- Transition Fault Model: The logic value of memory is not changed from '0' to '1' (upward transition), or '1' to 'O' (downward transition).
- Coupling Fault Model: The transition of logic value in one cell changes logic value of related cell's. [6].

A Register File Memory consists of a basic Memory Block (MB) of memory cells surrounded by ancillary circuitry to provide for access and synchronization. This circuitry includes Read and Write Address Buffers and Decoders, Input Data Latches, Output Data Buffers (normal and/or tristate), and a Clock Buffer. The memory cells consist of one or more bit storage locations as described later. The data cells can be written to by latching the data into an Input Dat Latch, the address to be written to into a Write Address Buffer, and enabling writing [9].

6 Hardware Implementation Design

To implement hardware we need to prepare circuit diagram and based on that one can start with PCB designing , listing out components , calculating cost , etc. In this project PCB designing software is used to make circuit diagram. This software also gives the actual image of printed circuit board. 8051 microcontroller is interfaced with 24c01 EEPROM IC and LCD display. LCD is interfaced on port0 while SCL and SDA pins of 24c01 EEPROM IC are connected to p1.0 and p1.1 pins of port1 respectively. Now all data pins of LCD are connected to port0 pins and pins RS, R/W and E are connected to pin numbers p2.0, p2.1 and p2.3 respectively.

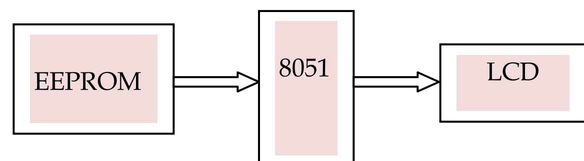
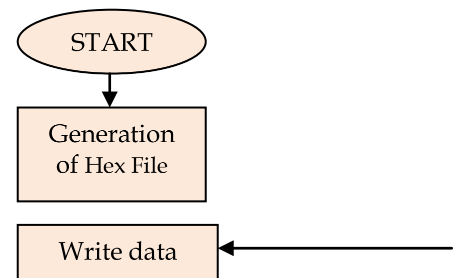


Fig.2. Block Diagram of Circuit

7 Software Implementation Design

The software framework is used to established communication between systems under test. To make communication USB to serial cable is used. Now as shown in above diagram we have to select controller and communication parameters. Once we finish with this we need to attach hardware kit through proper communication channel. Flow chart of process is mentioned in Figure number 3.



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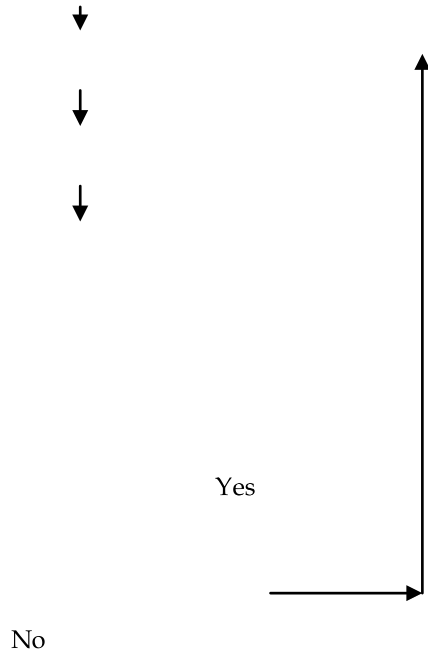

Fig.3. Flow chart for process

8 PROPOSED ARCHITECTURE PROCESS

The Evaluation parameter for proposed work is based on number of fault detected during one cycle of an instruction. Fault coverage refers to the percentage of some type of fault that can be detected during the test of any engineered system. High fault coverage is particularly valuable during manufacturing test and techniques such as Design for Test (DFT) and automatic test.

Pattern generations are used to increase it. In electronics for example, stuck-at fault coverage is measured by sticking each pin of the hardware model at logic '0' and logic '1', respectively, and running the test vectors. If at least one of the outputs differs from what is to be expected, the fault is said to be detected. Conceptually, the total number of simulation runs is twice the number of pins (since each pin is stuck in one of two ways, and both faults should be detected). However, there are many optimizations that can reduce the needed computation. In particular, often many non-interacting faults can be simulated in one run, and each simulation can be terminated as soon as a fault is detected. In this work EEPROM memory is tested successfully.

To carry this work, certain test cases are generated. The first test case consist of writing a a specific data in to each and every memory byte and simultaneously reading it out from the same memory locations and this data after reading will be stored in temporary register. Now data in temporary register is compared with the actual data which was written in to the memory. If this data is matched then memory byte location is ok otherwise not. Similarly second test case is generated but in this case master is writing and reading different data. Hence after successful completion of these test cases we can say that memory is tested successfully.

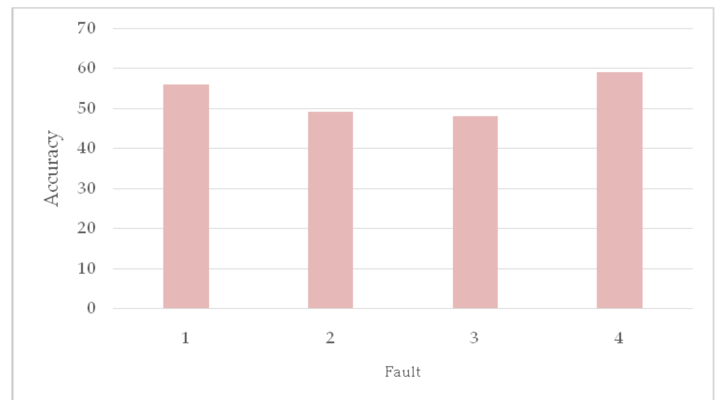

Fig.4. Output of Accuracy versus fault

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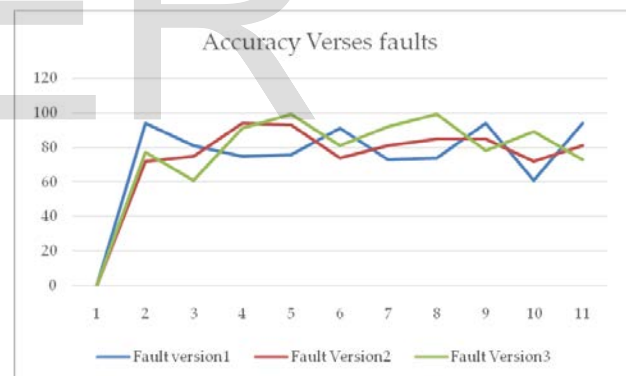

Fig.5. Accuracy versus faults in multiple versions

9 CONCLUSION

Importance of memory is increasing with the more and more increase in use of electronic devices. Online testing is an efficient mechanism to test memory of embedded systems.Accuracy verses faults graphs are calculated on the basis of test versions.With proposed approach memory can be efficiently tested tested as comparatively traditional approaches.

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